CLAIMS

What is claimed is:

1. A register file for a data processing system comprising:

a memory unit having a plurality of registers addresssable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode;

input ports to receive inputs for addressing at least one register using an encoded address; and

output ports to output data from at least register addressable by an encoded address.

2. The register file of claim 1, wherein the encoded address identifies a general purpose register associated with a processor mode.

3. The register file of claim 1, wherein each register is associated with a register index that maps to an encoded address based on at least one processor mode.

4. The register file of claim 3, wherein the input ports receive at least one source register index input and processor mode input for use in providing an encoded address for accessing at least one register.

5. The register file of claim 4, further comprising:

an address encoder, for each input port, the address encoder to provide an encoded address for accessing one of the plurality of registers.

6. The register file of claim 5, further comprising:

a latch to latch an encoded address from the address encoder; and

a selector coupled to the latch and the address encoder, the selector to select the encoded address from either the latch or the address encoder.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

7. The register file of claim 6, wherein the latch stores the encoded address as a pipeline storage of the encoded address.

8. The register file of claim 4, wherein data for one or more instructions being processed is outputted from the memory unit.

9. The register file of claim 3, further comprising:

input ports to receive at least one write index input and processor mode input for use in providing the encoded address for writing data to at least one register; and

at least one write input port for writing the data to the register addressable by the encoded address.

10. The register file of claim 9, wherein data for one or more executed instructions for the data processing are written into the memory unit.

11. The register file of claim 3, wherein the processor mode includes exception handling modes.

12. The register file of claim 11, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction (UND), and abort exception (ABT) mode.

13. The register file of claim 12, wherein each exception handling mode corresponds to one or more registers.

14. A register file for a data processing system comprising:

a memory means having a plurality of register means addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of register means and a corresponding processor mode;

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

input means for receiving inputs for addressing at least one register means using an encoded address; and

output means for outputting data from at least one register means addressable by an encoded address.

15. The register file of claim 14, wherein the encoded address identifies a general purpose register associated with a processor mode.

16. The register file of claim 14, wherein each register means is associated with a register index that maps to an encoded address based on at least one processor mode.

17. The register file of claim 16, wherein the input means further includes means for receiving at least one source register index input and processor mode input for use in providing an encoded address for accessing at least register means.

18. The register file of claim 17, further comprising:

addressing means for providing an encoded address to address one of the plurality of register means.

19. The register file of claim 18, further comprising:

a latching means for latching an encoded address from the address encoder; and

a selecting means coupled to the latching means and the addressing means for selecting the encoded address from either the latching means or the addressing means.

20. The register file of claim 19, wherein the latching means includes storage means for storing the encoded address as a pipeline storage of the encoded address.

21. The register file of claim 17, wherein data for one or more instructions being processed is outputted from the memory means.

22. The register file of claim 16, further comprising:

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

input means for receiving at least one write index input and processor mode input for use in providing the encoded address for writing data to at least one register means; and

at least one write input means for writing the data to the register means addressable by the encoded address.

23. The register file of claim 22, wherein data for one or more executed instructions for the data processing are written into the memory means.

24. The register file of claim 16, wherein the processor mode includes exception handling modes.

25. The register file of claim 24, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction (UND) mode, and abort exception (ABT) mode.

26. The register file of claim 25, wherein each exception handling mode corresponds to one or more register means.

27. A data processing system comprising:

a microprocessor comprising:

a plurality of pipeline stages including a register file, the register file including:

a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode;

input ports to receive inputs for addressing at least one register using an encoded address; and

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

output ports to output data from at least one register addressable by an encoded address.

28. The data processing system of claim 27, wherein the encoded address identifies a general purpose register associated with a processor mode.

29. The data processing system of claim 27, wherein the pipeline stages include:

an instruction fetch stage to fetc one or more instructions; and

an instruction decode stage to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the memory unit for outputting data from or writing data to one or more of the registers.

30. The data processing system of claim 29, wherein the register file further includes:

a plurality of input ports to receive inputs from the instruction decode stage, the inputs being used to obtain the encoded address for accessing at least one register; and

at least one output port to output data from the register addressable by the encoded address.

31. The data processing system of claim 30, wherein the pipeline stages further include:

an execution stage including a plurality of execution units, each execution unit to receive data from the register file for executing an instruction.

32. The data processing system of claim 31, further comprising:

a write back or retire logic stage to receive results data associated with one or more instructions executed by the execution units of the execution stage, and to forward the results data to the register file for storage.

33. The data processing system of claim 32, wherein the register file further includes:

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

a plurality of input ports to receive the data from the write back or retire logic for one or more executed instructions, the data to be written in the register file.

34. The data processing system of claim 29, wherein each register is associated with a register index that maps to one of the encoded addresses based on at least one processor mode.

35. The data processing system of claim 34, wherein the processor mode includes exception handling modes.

36. The data processing system 35, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction mode (UND), and abort exception (ABT) mode.

37. The data processing system of claim 36, wherein each exception handling mode corresponds to one or more registers.

38. A data processing system comprising:

a processing means for processing instructions:

a pipeline means for executing instructions, the pipeline means including a register file means, the register file means including:

a memory means having a plurality of register means addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of register means and a corresponding processor mode.

input means for receiving inputs for addressing at least one register means using an encoded address; and

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

output means for outputting output data from at least one register means addressable by an encoded address.

39. The register file of claim 38, wherein the encoded address identifies a general purpose register associated with a processor mode.

40. The data processing system of claim 38, wherein the pipeline means includes:

a fetching means for fetching one or more instructions for execution; and

decoding means for decoding fetched instructions from the fetching means and for forwarding inputs to the memory means for outputting data from or writing data to one or more of the register means.

41. The data processing system of claim 40, wherein the register file means further includes:

input means for receiving inputs from the decoding means, the inputs being used to obtain the encoded address for accessing at least one register; and

at least one output means for outputting data from the register addressable by the encoded address.

42. The data processing system of claim 41, wherein the pipeline means further includes:

an execution means including a plurality of execution processing means, each execution processing means receiving receive data from the register file means for executing an instruction.

43. The data processing system of claim 42, further comprising:

a write back means or retire logic means for receiving results data associated with one or more instructions executed by an execution processing means and for forwarding the results data to the register file means for storage.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

44. The data processing system of claim 43, wherein the register file means further includes:

a plurality of input means for receiving the data from the write back means or retire logic means for one or more executed instructions, the data to be written in the register file means.

45. The data processing system of claim 40, wherein each register means is associated with a register index that maps to one of the encoded addresses based on at least one processor mode.

46. The data processing system of claim 45, wherein the processor mode includes exception handling modes.

47. The data processing system 46, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction (UND) mode, and abort exception (ABT) mode.

48. The data processing system of claim 47, wherein each exception handling mode corresponds to one or more register means.

49. A microprocessor comprising:

an integrated circuit comprising:

a memory unit having a plurality of registers addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode; and

at least one address encoder to provide at least one encoded address for addressing at least one of the registers.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

50. The microprocessor of claim 49, wherein the encoded address identifies a general purpose register associated with a processor mode.

51. The microprocessor of claim of claim 49, wherein each register is associated with a register index that maps to the encoded address based on at least one processor mode.

52. The microprocessor of claim 51, wherein the processor mode includes exception handling modes.

53. The microprocessor of claim 52, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction (UND) mode, and abort exception (ABT) mode.

54. The microprocessor of claim 51, further comprising:

at least one input to receive index and processor mode information for use in providing the encoded address; and

at least one output to output data stored in the storage location addressable by the encoded address.

55. The microprocessor of claim 51, further comprising:

at least one input to receive index and processor mode information for use in providing the encoded address; and

at least one write input to receive data to be written into the storage location addressable by the encoded address.

56. A data processing system comprising a memory mapped register file for accessing a plurality of registers using an encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

57. A microprocessor comprising:

an integrated circuit means comprising:

a memory means having a plurality of register means addressable by an encoded address, wherein the encoded address corresponds to a respective one of the plurality of register means and a corresponding processor mode; and

at least one addressing means for providing at least one encoded address for addressing at least one of the register means.

58. The microprocessor of claim 57, wherein the encoded address identifies a general purpose register associated with a processor mode.

59. The microprocessor of claim of claim 57, wherein each register means is associated with a register index that maps to the encoded address based on at least one processor mode.

60. The microprocessor of claim 59, wherein the processor mode includes exception handling modes.

61. The microprocessor of claim 60, wherein the exception handling processor modes include at least one of a fast interrupt request (FIQ) mode, interrupt request (IRQ) mode, supervisor (SVC) mode, undefined instruction (UND) mode, and abort exception (ABT) mode.

62. The microprocessor of claim 61, wherein the exception handling modes correspond to one or more registers.

63. The microprocessor of claim 59, further comprising:

at least one input means for receiving index and processor mode information for use in providing the encoded address; and

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

at least one output means for outputting data stored in the storage location addressable by the encoded address.

64. The microprocessor of claim 59, further comprising:

at least one input means for receiving index and processor mode information for use in providing the encoded address; and

at least one write input means for receiving data to be written into the storage location addressable by the encoded address.

65. An integrated circuit method comprising:

configuring the integrated circuit to receive processor mode and source data inputs;

configuring the integrated circuit to determine an encoded address based on the processor mode and source data inputs, wherein the encoded address corresponds to a respective one of a plurality of registers and a corresponding processor mode;

configuring the integrated circuit to address one of the registers using an encoded address; and

configuring the integrated circuit to output data from the register addressable by the encoded address.

66. The method of claim 65, further comprising:

configuring the integrated circuit to output data for multiple instructions.

67. The method of claim 65, further comprising:

configuring the integrated circuit to write data to one of the registers addressable by an encoded address.

68. The method of claim 67, further comprising:

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

configuring the integrated circuit to write data to one or more registers for multiple executed instructions.

69. A method for accessing a memory unit having a plurality of registers comprising:

receiving inputs for accessing the register file;

determining at least one encoded address in accordance with the received inputs;

accessing the memory unit in accordance with the encoded address, wherein the encoded address corresponds to a respective one of the plurality of registers and a corresponding processor mode; and

outputting data from the memory unit accessed with the encoded address.

70. The method of claim 69, wherein receiving the inputs includes receiving processor mode inputs and source data inputs.

71. The method of claim 70, wherein determining at least one encoded address includes determining at least one encoded address based on the processor mode inputs and source data inputs.

72. The method of claim 69, wherein outputting data includes outputting data for multiple instructions.

73. The method of claim 69, further comprising:

writing data to at least one of the registers addressable by the encoded address.

74. The method of claim 73, further comprising:

writing write data to the registers for multiple executed instructions.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com